CLAIMS:

1. A method for creating an architecture of a reconfigurable logic core on an integrated circuit, the architecture comprising logic components, routing components and interface components, characterized in that the architecture is derived from a template, the template being a model configured by a plurality of parameters, wherein the model defines the logic components, the routing components and the interface components, the parameters having values and the values being in accordance with an application domain.

2. A method as claimed in claim 1, wherein the template comprises an array, the array comprising a plurality of logic tiles, and the number of logic tiles being a first parameter.

3. A method as claimed in claim 2, the aspect ratio of the array being a second parameter.

4. A method as claimed in claim 3, wherein the template further comprises:

- at least one simple input/output tile, the simple input/output tile being coupled to a first logic tile;
- at least one input/output tile with routing functionality, the input/output tile with routing functionality being coupled to a second logic tile;
- a corner routing tile, the corner routing tile being coupled to at least two input/output tiles.

5. A method as claimed in claim 4, wherein at least one of the logic tiles comprises:

- a logic block, the logic block comprising a plurality of logic block ports;
- routing resources, the routing resources comprising:
  - a plurality of routing tracks;
  - logic ports, the logic ports being arranged to couple the logic block ports to a neighboring logic tile;

- routing ports, the routing ports being arranged to couple the routing tracks to a neighboring logic tile;

- direct ports, the directs ports enabling a direct connection of the logic block with neighboring logic tiles.

6. A method as claimed in claim 5, wherein the logic block ports comprise first primary input ports and the logic block further comprises:

- a plurality of processing clusters, the number of processing cluster being a third parameter, wherein at least one of the processing clusters comprises a plurality of serially connected processing elements, the number of processing elements being a fourth parameter, and the processing cluster further comprising a plurality of first secondary input ports, a first carry input port and a first carry output port;

- a first multiplexer block, the first multiplexer block being arranged to be controlled by control signals issued by a first input selection block, the first multiplexer block being arranged to make a selection from first intermediate signals issued by the processing elements;

- an output selection block, the output selection block being arranged to receive the selection of the first intermediate signals and to determine the number of output signals of the logic block, the output selection block further being arranged to generate the output signals and to send the output signals to output ports of the logic block;

- a flip-flop block, the flip-flop block being arranged to register the output signals.

7. A method as claimed in claim 6, wherein the first input selection block is arranged to couple the first primary input ports to second primary input ports, the second primary input ports being comprised in the processing elements, and to select input signals; the first input selection block further being arranged to accept output signals of the logic block as input signals such that a feedback loop is realized.

8. A method as claimed in claim 6, wherein at least one of the processing elements comprises:

- a plurality of serially connected logic elements, the number of logic elements being a fifth parameter;

- the second primary input ports;

- a plurality of second secondary input ports, the second secondary input ports being coupled to third secondary input ports comprised in the logic elements;
- a second carry input port, the second carry input port being coupled to a third carry input port comprised in a first one of the serially connected logic elements;
- a second carry output port, the second carry output port being coupled to a third carry output port comprised in a last one of the serially connected logic elements;
- a plurality of first arithmetic output ports;
- a first Boolean output port;
- a second input selection block, the second input selection block being arranged to couple the second primary input ports to third primary input ports comprised in the logic elements, and to select input signals;
- a second multiplexer block, the second multiplexer block being arranged to be controlled by control signals issued by the second input selection block, the second multiplexer block being arranged to select signals originating from second Boolean output ports comprised in the logic elements, and the second multiplexer block further being arranged to produce an output signal for the first Boolean output port;
- wherein second arithmetic output ports comprised in the logic elements are coupled to the first arithmetic output ports.

9. A method as claimed in claim 8, wherein at least one of the logic elements comprises:
- a plurality of third primary input ports, the number of third primary input ports being a sixth parameter;
- the third carry input port or a further carry input port;
- the third carry output port or a further carry output port;
- one of the second Boolean output ports;
- a plurality of the second arithmetic output ports, the number of second arithmetic output ports being a seventh parameter.

10. A reconfigurable logic core having an architecture created by a method as claimed in any of the preceding claims.